The **“Generate”** option allows the user to select the different views that can be generated. By default the compiler generates all the views. If the user wants to generate only timing views, he/she can deselect the **“ALL”** button. Timing views are always generated. If the aim is to find out the optimum configuration, the user can generate the timing views only. Based on the access time and the area from the datasheet, the user can decide to generate other views. The different views available in the compiler are **Netlist, Gds, Lef, Verilog, ATPG, MBIST, Logic Vision** and **Timing**. The user can generate all the views for a memory instance in less than a minute. Depending on the requirements, different views are added to the compiler from time to time. The compiler also generates the **“Antenna Lef”**.